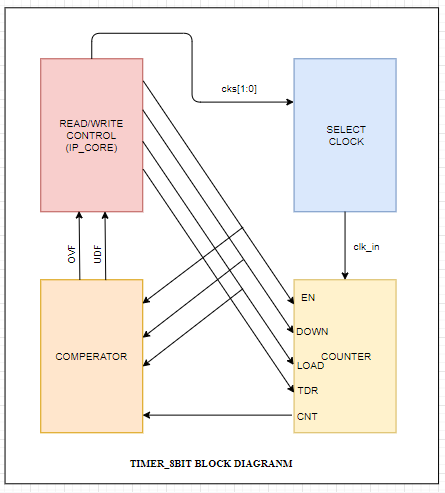
**TIMER 8 BIT SPECIFICATION**

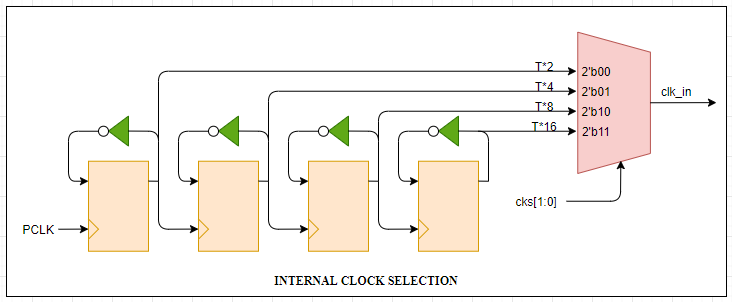
**I/ Block Diagram**

**1. Timer 8 bit block diagram**

****

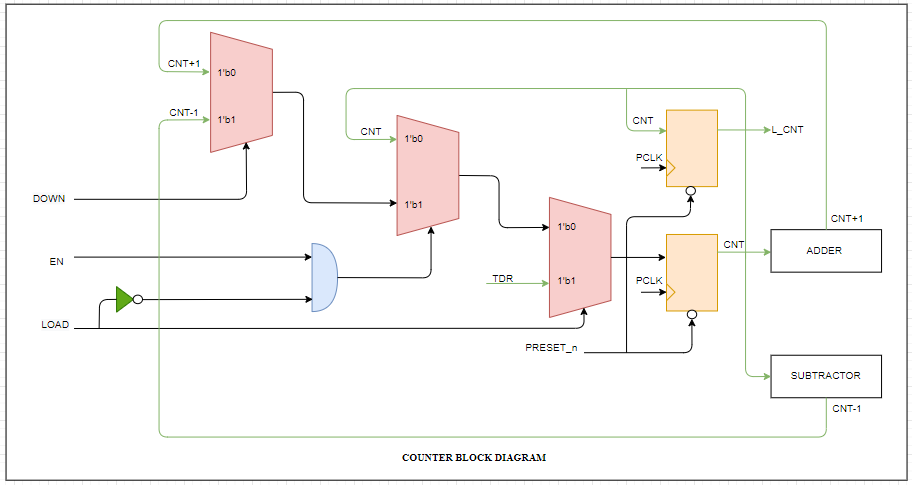
**Figure 1.1. Timer 8 bit block diagram**

**2. Internal clock selection**

****

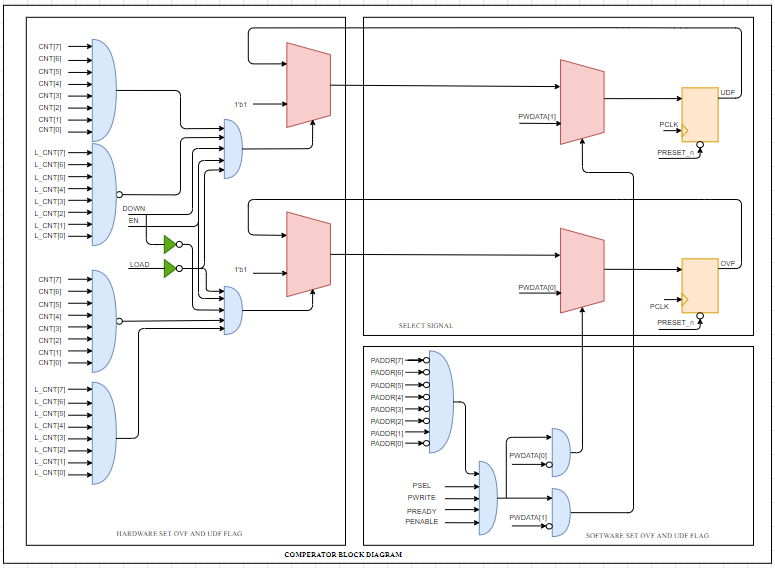
**Figure 1.2. Clock Generator block diagram**

**3. Counter**

****

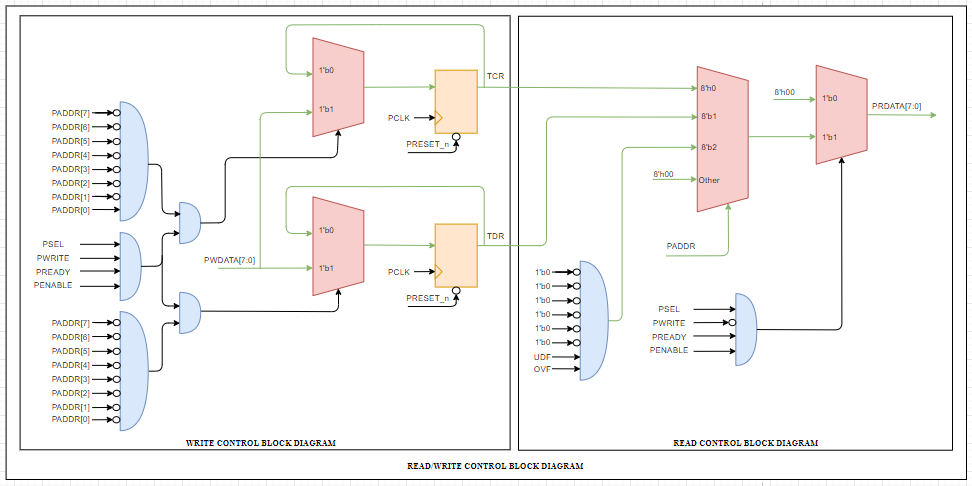
**Figure 1.3. Counter 8 bit block diagram**

**4. Comperator**

****

**Figure 1.4. Comperator block diagram**

**5. Read/Write control**

****

**Figure 1.5. Read/Write control block diagram**

**II/ Register table**

**1. TDR[7:0] – Address 8’h00:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **TDR[7:0]** | | | | | | | |
| **Bit 7** | **Bit 6** | **Bit 5** | **Bit 4** | **Bit 3** | **Bit 2** | **Bit 1** | **Bit 0** |
| TDR[7] | TDR[6] | TDR[5] | TDR[4] | TDR[3] | TDR[2] | TDR [1] | TDR [0] |

**2. TCR[7:0] – Address 8’h01:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **TCR[7:0]** | | | | | | | |
| **Bit 7** | **Bit 6** | **Bit 5** | **Bit 4** | **Bit 3** | **Bit 2** | **Bit 1** | **Bit 0** |
| LOAD | Reserved | DOWN | EN | Reserved | Reserved | CKS[1] | CKS[0] |

*Table 2.1. Function table for TCR[7:0]*

|  |  |  |
| --- | --- | --- |
| **Bit name** | **R/W** | **Description** |
| Load[7] | R/W | Manual load data from TDR to TCNT when it active High. 1: load data to TCNT 0: Normal operation. |
| 6 | Reserved | Reserved |
| Up/Dw[5] | R/W | Control counter up or counter down 0: counter up 1: counter down |
| En[4] | R/W | 0 : disable 1: enable |
| 3:2 | Reserved | Reserved |
| cks[1:0] | R/W | Select internal clocks for circuit 00 : T\*2 01 : T\*4 10 : T\*8 11: T\*16 |

**3. TSR[7:0] – Address 8’h02:**

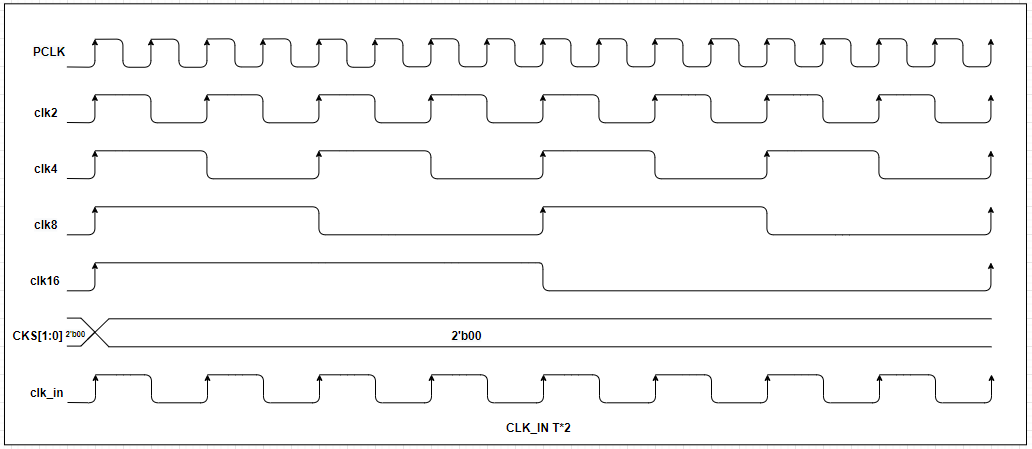
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **TSR[7:0]** | | | | | | | |
| **Bit 7** | **Bit 6** | **Bit 5** | **Bit 4** | **Bit 3** | **Bit 2** | **Bit 1** | **Bit 0** |
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | UDF | OVF |

*Table 2.2. Function table for TSR[7:0]*

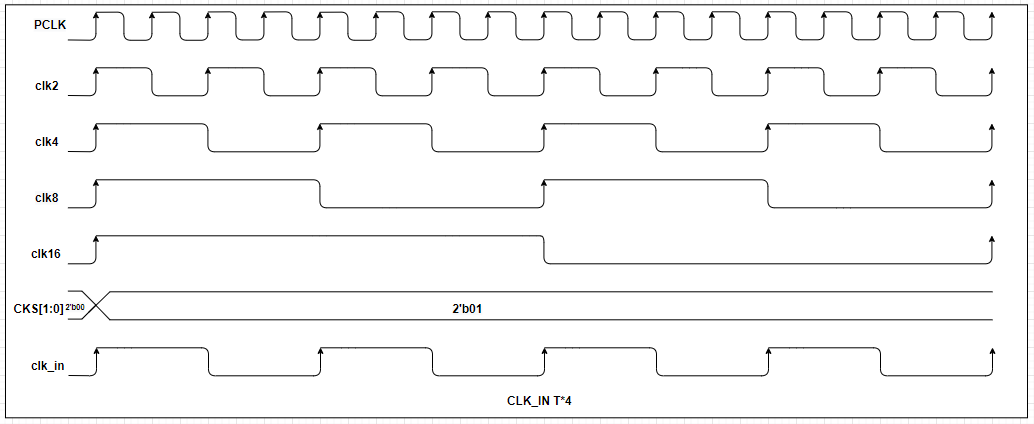
|  |  |  |
| --- | --- | --- |
| **Bit name** | **R/W** | **Description** |
| 7:2 | R | Reserved |
| UDF[1] | R/W\* | Timer counter underflow when counter 8’h00 down to 8’hff: This bit is only set by hardware, clear by software |
| OVF[0] | R/W\* | Timer counter overflow when counter 8’hFF to 8’h00: This bit is only set by hardware, clear by software |

**III/ Timing chart**

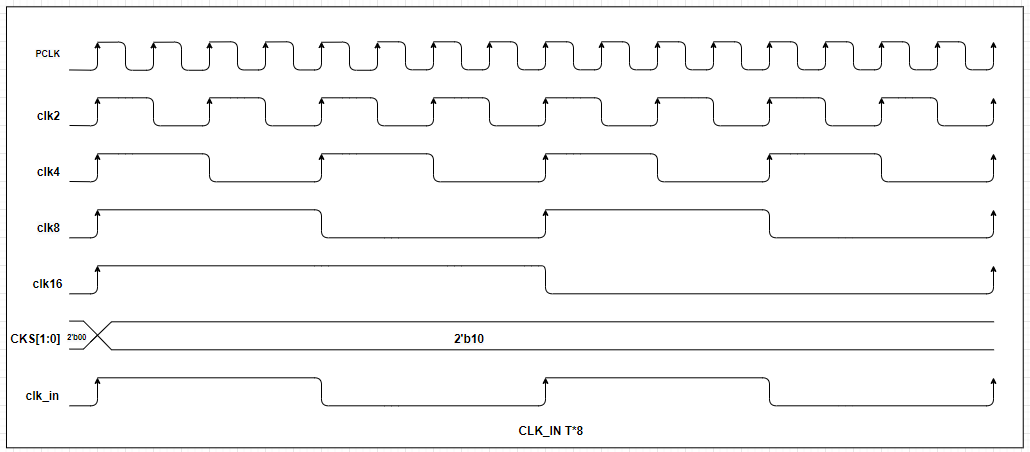
**3.1. Timing char for Clock Generator**

****

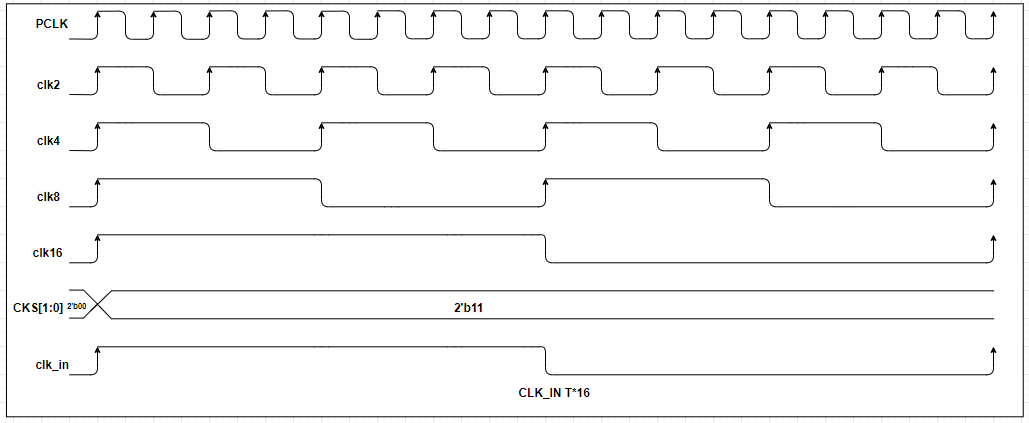
**Figure 3.1. Timing chart for clk\_in T\*2**

****

**Figure 3.2. Timing chart for clk\_in T\*4**

****

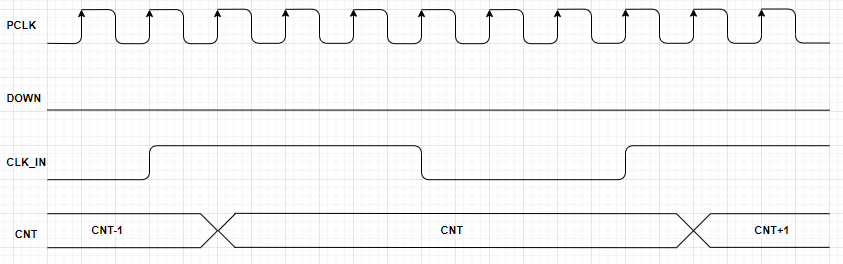
**Figure 3.3. Timing chart for clk\_in T\*8**

****

**Figure 3.4. Timing chart for clk\_in T\*16**

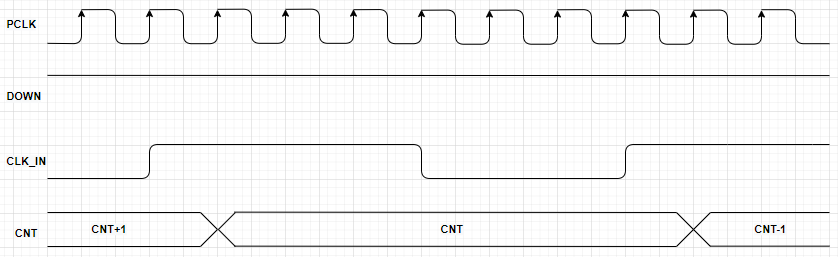
**3.2. Timing char for Counters and Flags**

**1. Counter up**

****

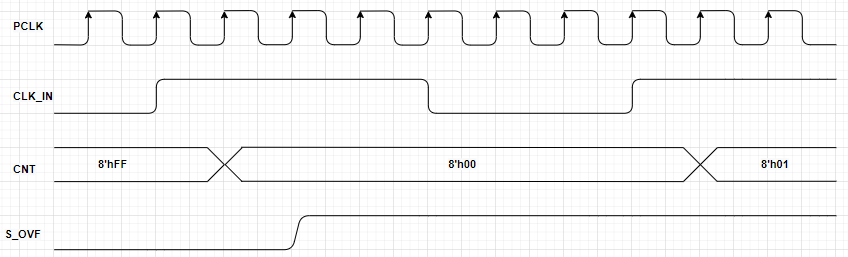
**Figure 3.5. Timing char for counter up**

**2. Counter down**

****

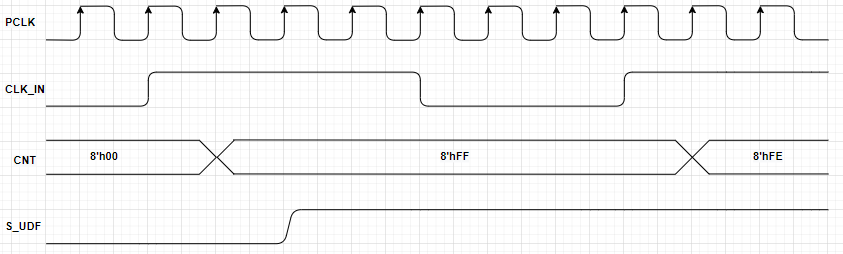
**Figure 3.6. Timing char for counter down**

**3. Overflow**

****

**Figure 3.7. Timing char for overflow**

**4. Underflow**

****

**Figure 3.8. Timing char for underflow**

**IV/ IF Table**

**1. Read/Write control**

*Table 4.1. IF table for R/W control*

|  |  |  |
| --- | --- | --- |
| **Portname** | **I/O** | **Decriptrion** |
| PCLK | Input | System clock for Timer 8-bit |
| PRESET | Input | System reset for Timer 8-bit |
| PENABLE | Input | Enable Timer 8-bit |
| PSEL | Input | Select signal from APB bus |
| PREADY | Input | Ready signal from APB bus |
| PWRITE | Input | Write signal from APB bus |
| PADDR[7:0] | Input | ADDR from APB bus |
| PWDATA[7:0] | Input | Data write from APB bus |

**2. Clock Generator**

*Table 4.2. IF table clock generator*

|  |  |  |
| --- | --- | --- |
| **Portname** | **I/O** | **Decriptrion** |
| PCLK | Input | System clock for Timer 8-bit |
| PRESET | Input | System reset for Timer 8-bit |
| PENABLE | Input | Enable Timer 8-bit |
| CKS[1:0] | Input | Select Internal Clock |
| clk2 | Input | T\*2 |
| clk4 | Input | T\*4 |
| clk8 | Input | T\*8 |
| clk16 | Input | T\*16 |
| clk\_in | Output | Input clock for Timer 8-bit activities |

**3. Counter for Timer 8-bit**

*Table 4.3. IF table for counter*

|  |  |  |
| --- | --- | --- |
| **Portname** | **I/O** | **Decriptrion** |
| PCLK | Input | System clock. Use for update values of CNT |
| clk\_in | Input | Clock for Timer 8-bit |
| PRESET | Input | System reset for Timer 8-bit |
| TDR[7:0] | Input | Timer Data Register, supply values for CNT when LOAD=1 |
| EN | Input | Enable counter |
| LOAD | Input | Load data from TDR to CNT register |
| DOWN | Input | Up/Down select |
| CNT[7:0] | Output | Internal value counter register |
| L\_CNT[7:0] | Output | Last\_counter register. Contain the previous values of CNT register |

**4. Comperator for Timer 8-bit**

*Table 4.4. IF table for comperator*

|  |  |  |
| --- | --- | --- |
| **Portname** | **I/O** | **Decriptrion** |
| PCLK | Input | System clock for Timer 8-bit |
| PRESET | Input | System reset for Timer 8-bit |
| PENABLE | Input | Enable Timer 8-bit |
| PSEL | Input | Select signal from APB bus |
| PREADY | Input | Ready signal from APB bus |
| PWRITE | Input | Write signal from APB bus |
| PADDR[7:0] | Input | ADDR from APB bus |
| PWDATA[7:0] | Input | Data write from APB bus |
| EN | Input | Enable counter |
| LOAD | Input | Load data from TDR to CNT register |
| DOWN | Input | Up/Down select |
| CNT[7:0] | Input | Internal counter register |
| L\_CNT[7:0] | Input | Last\_counter register. Contain the previous values of CNT register |
| OVF | Output | Overflow flag for timer 8-bit. Set by **hardware** but only clear by **software**. |
| UDF | Output | Underflow flag for timer 8-bit. Set by **hardware** but only clear by **software**. |